

**ABSTRACT OF THE DISCLOSURE**

A zero-power electrically erasable and programmable memory cell is implemented in CMOS (complementary metal oxide semiconductor) technology. A P-channel sense transistor has a source coupled to a first voltage generator, and an N-channel sense transistor has a source coupled to a second voltage generator. The drains of the P-channel and N-channel sense transistors are coupled together to form an output of the memory cell, and the gates of the P-channel and N-channel sense transistor are coupled together to form a floating gate of the memory cell. In an example embodiment of the present invention, each of the first and second voltage generators are variable voltage generators that apply a positive voltage at the respective source of each of the P-channel and N-channel sense transistors during the erase operation and/or that apply a ground or negative voltage at the respective source of each of the P-channel and N-channel sense transistors during the program operation. In another embodiment of the present invention, a magnitude of the respective threshold voltage of each of the P-channel and N-channel sense transistors is higher than a magnitude of a threshold voltage of standard process P-channel and N-channel transistors. With such a higher threshold voltage, the P-channel and N-channel sense transistors do not erroneously turn on to dissipate power during the read operation, to ensure that the memory cell is a zero-power memory cell.